

FIG. 1

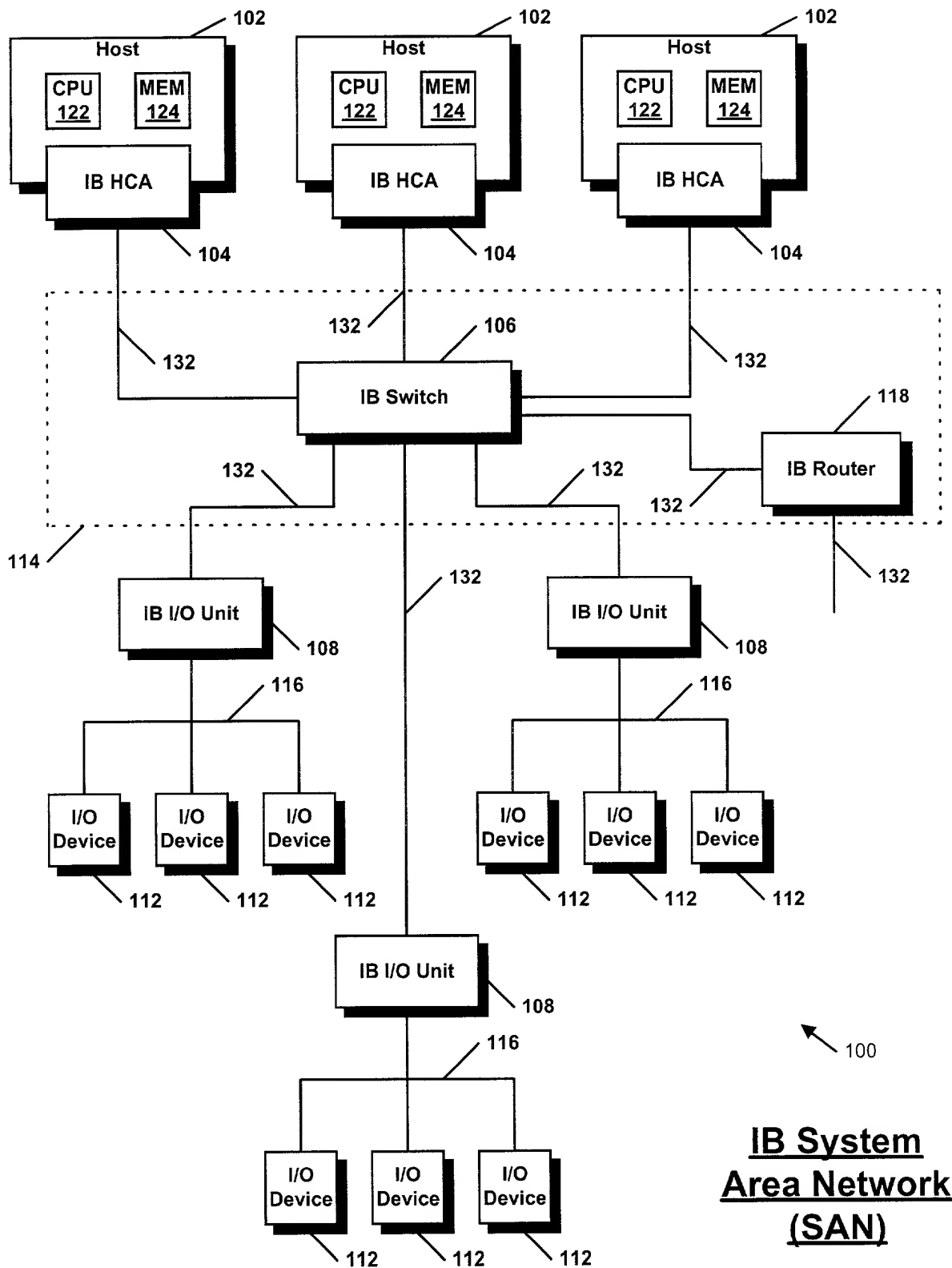
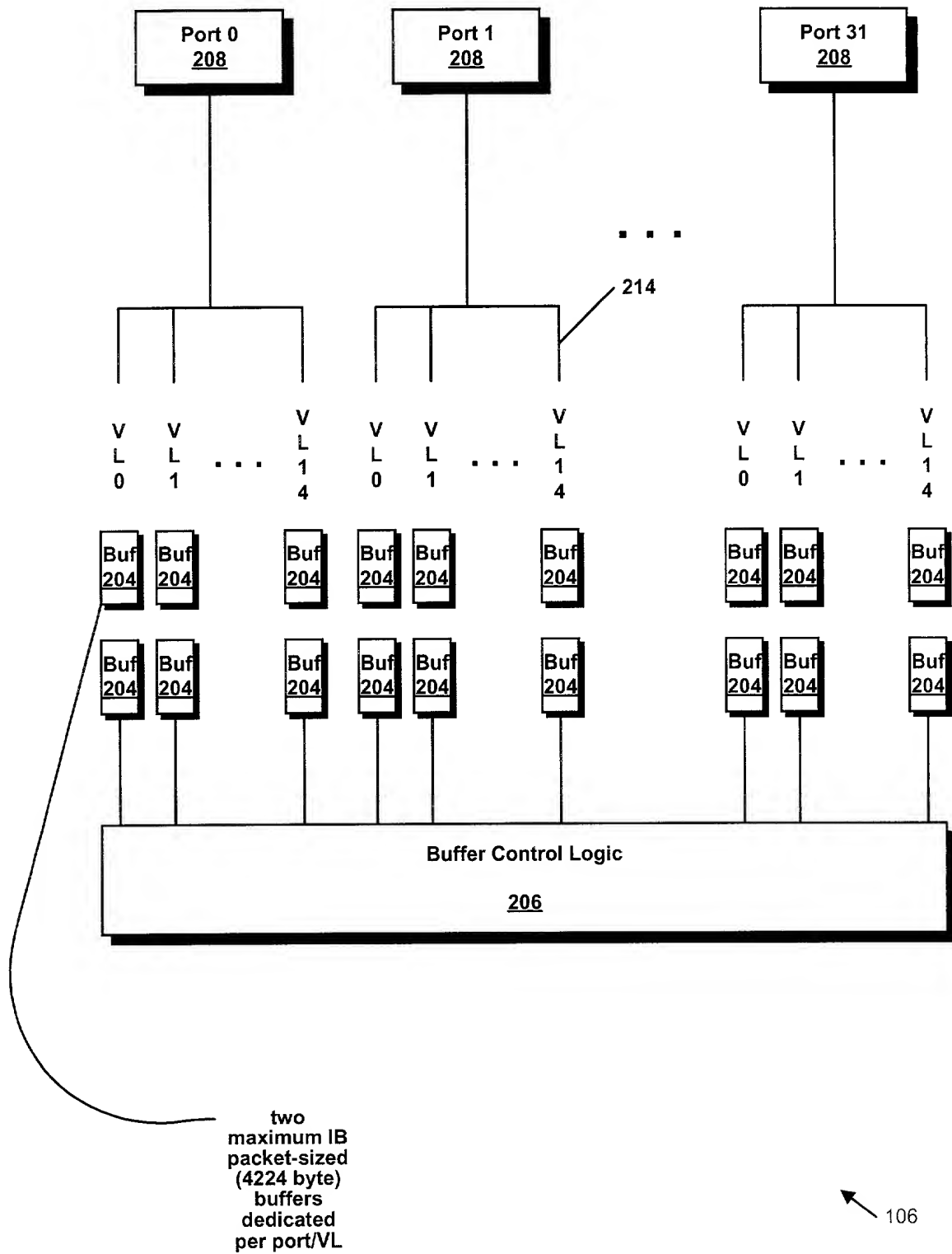
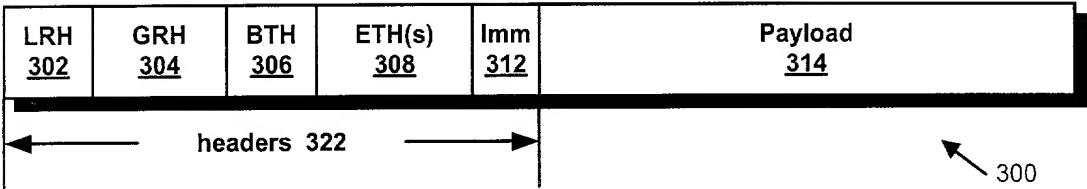


FIG. 2 (Related Art)



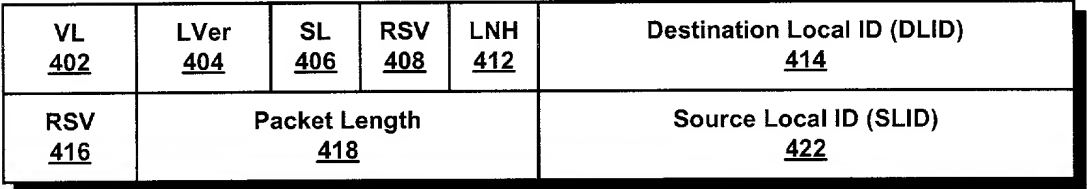
Conventional IB Switch

FIG. 3 (Related Art)



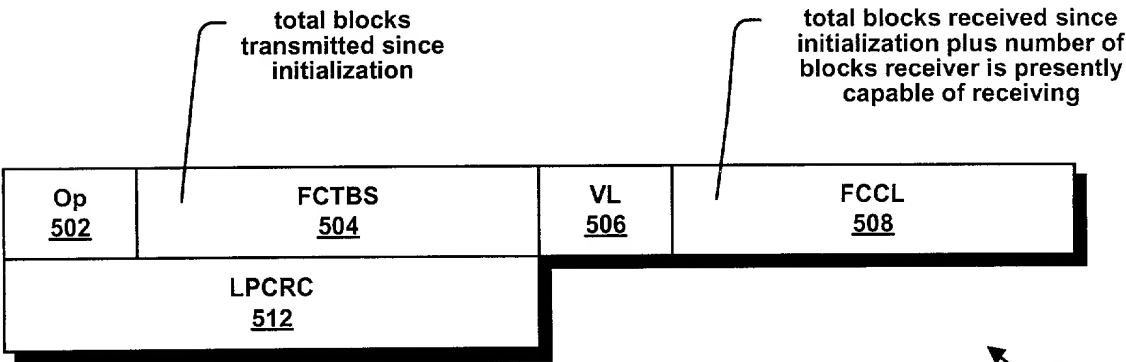
IB Data Packet

FIG. 4 (Related Art)



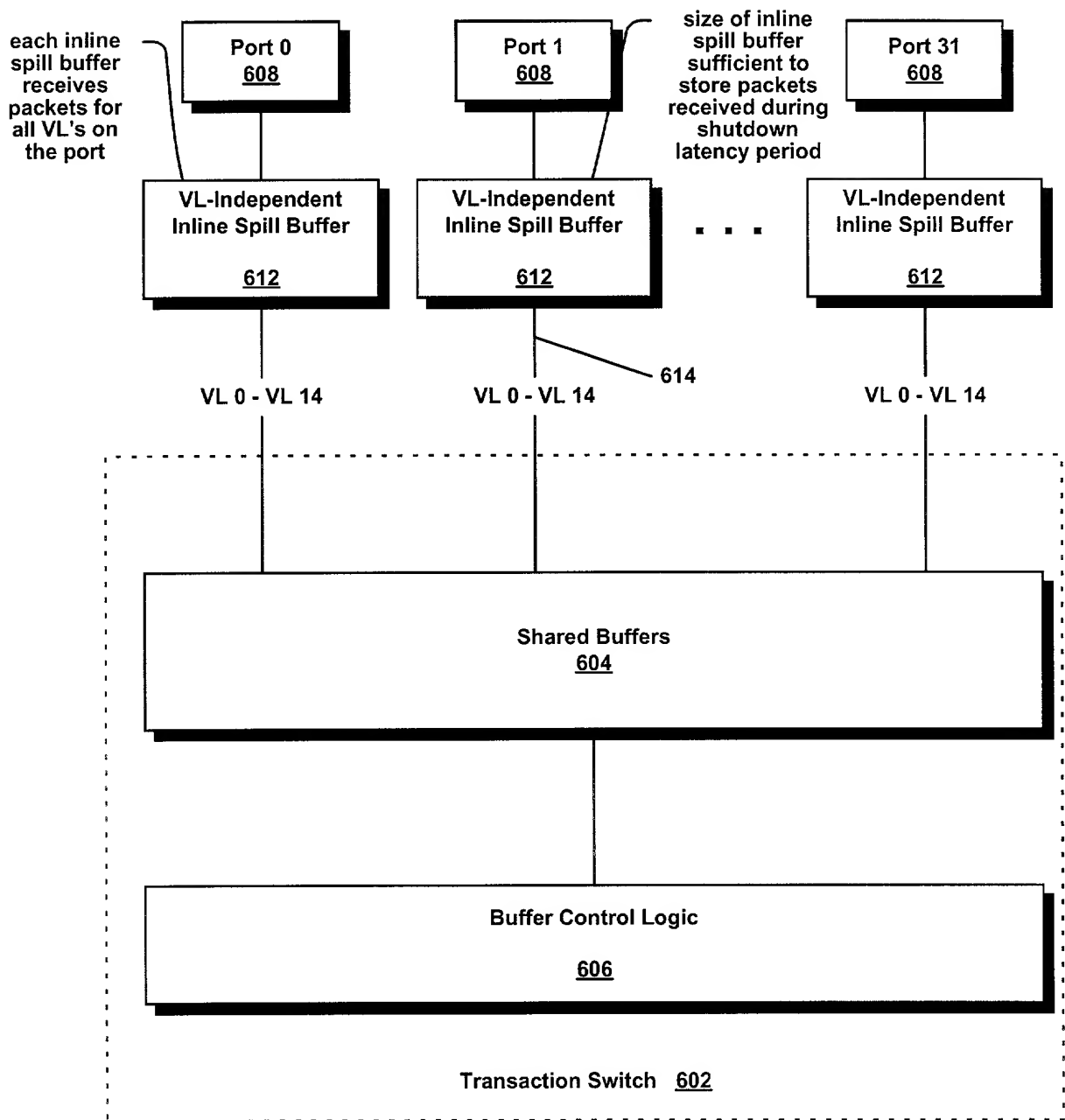
Local Routing Header

FIG. 5 (Related Art)



Flow Control Packet

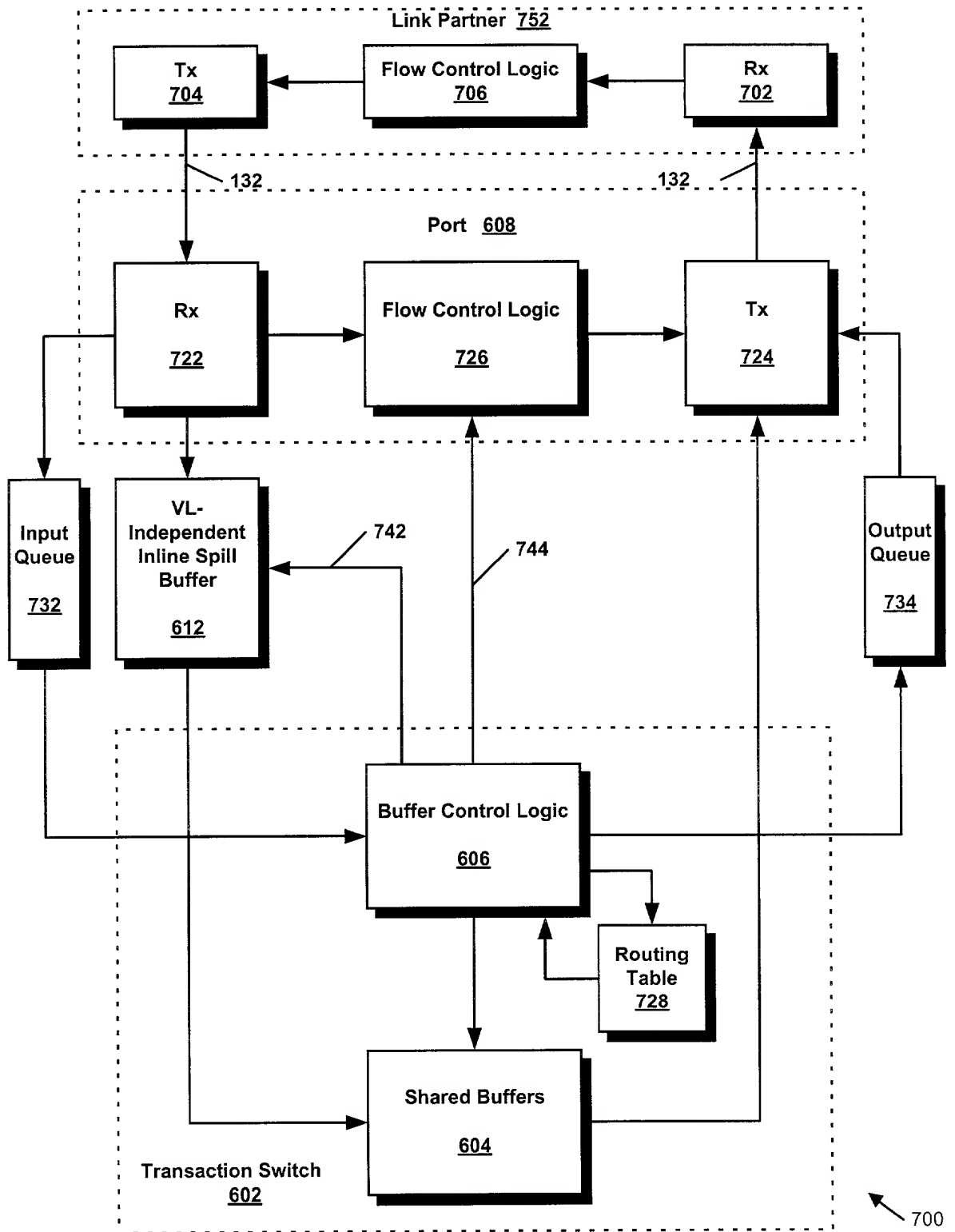
FIG. 6



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IB Switch Capable of Over-Advertising Buffering Resources Using Inline Spill Buffer

FIG. 7



Packet Buffering System Using Inline Spill Buffer

FIG. 8



Valid	Good Packet	VL	GRH present	DLID	SLID	Packet Length	Destination QP
<u>802</u>	<u>804</u>	<u>806</u>	<u>808</u>	<u>812</u>	<u>814</u>	<u>816</u>	<u>818</u>

Input Queue Entry

800

FIG. 9

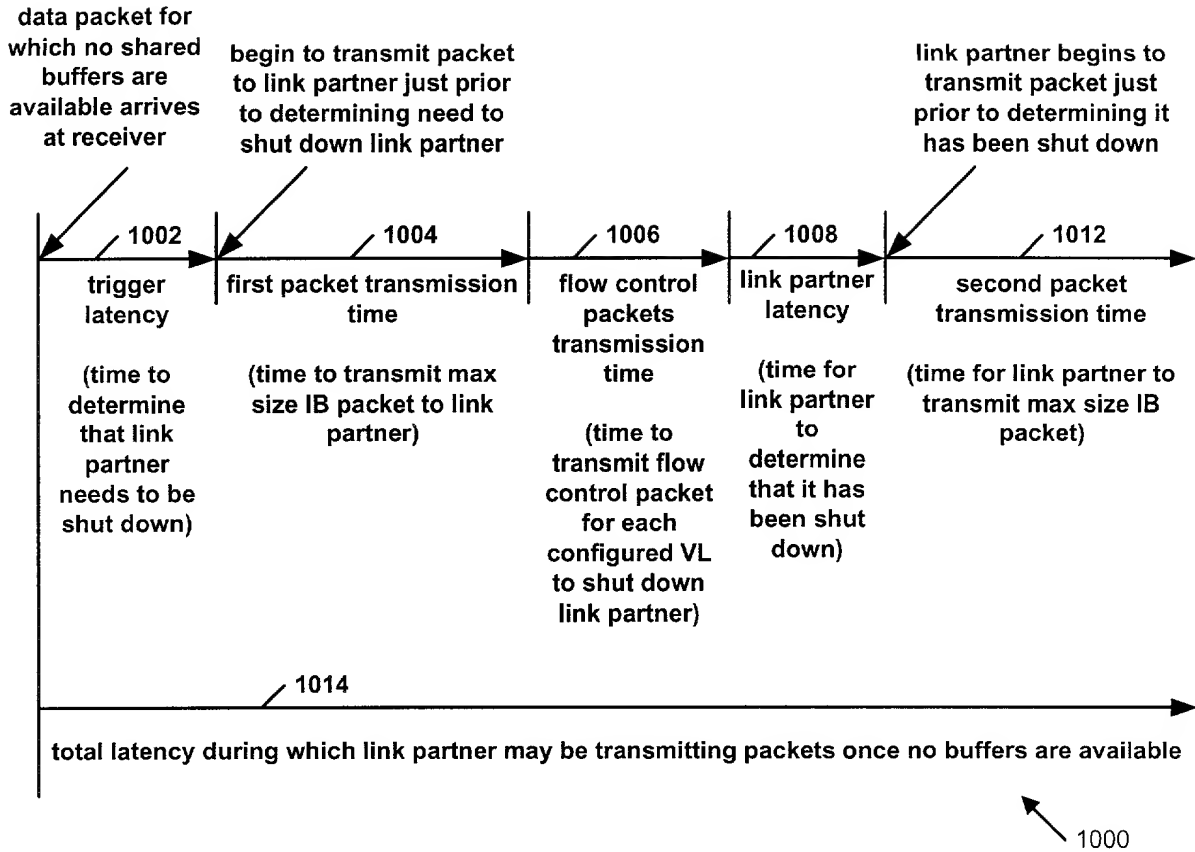
Tag	VL	Packet Length	Chunk Address 0	Chunk Address 1	Chunk Address 2	Chunk Address 3	Chunk Address 4	Chunk Address 5
<u>902</u>	<u>904</u>	<u>906</u>	<u>908</u>	<u>912</u>	<u>914</u>	<u>916</u>	<u>918</u>	<u>922</u>

Output Queue Entry

900

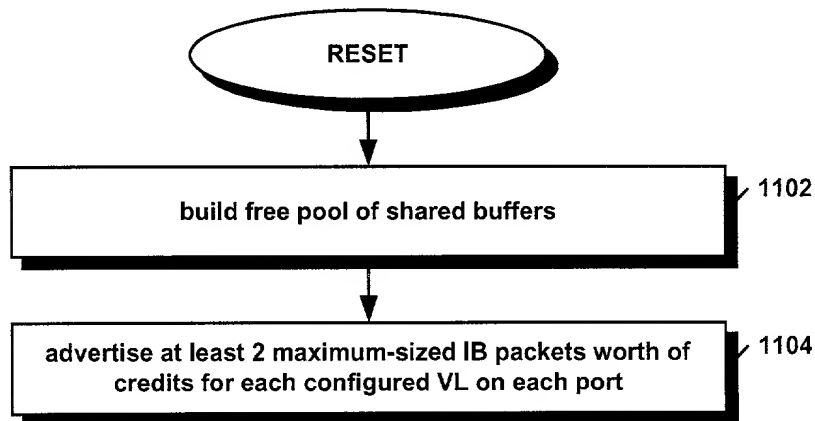


FIG. 10



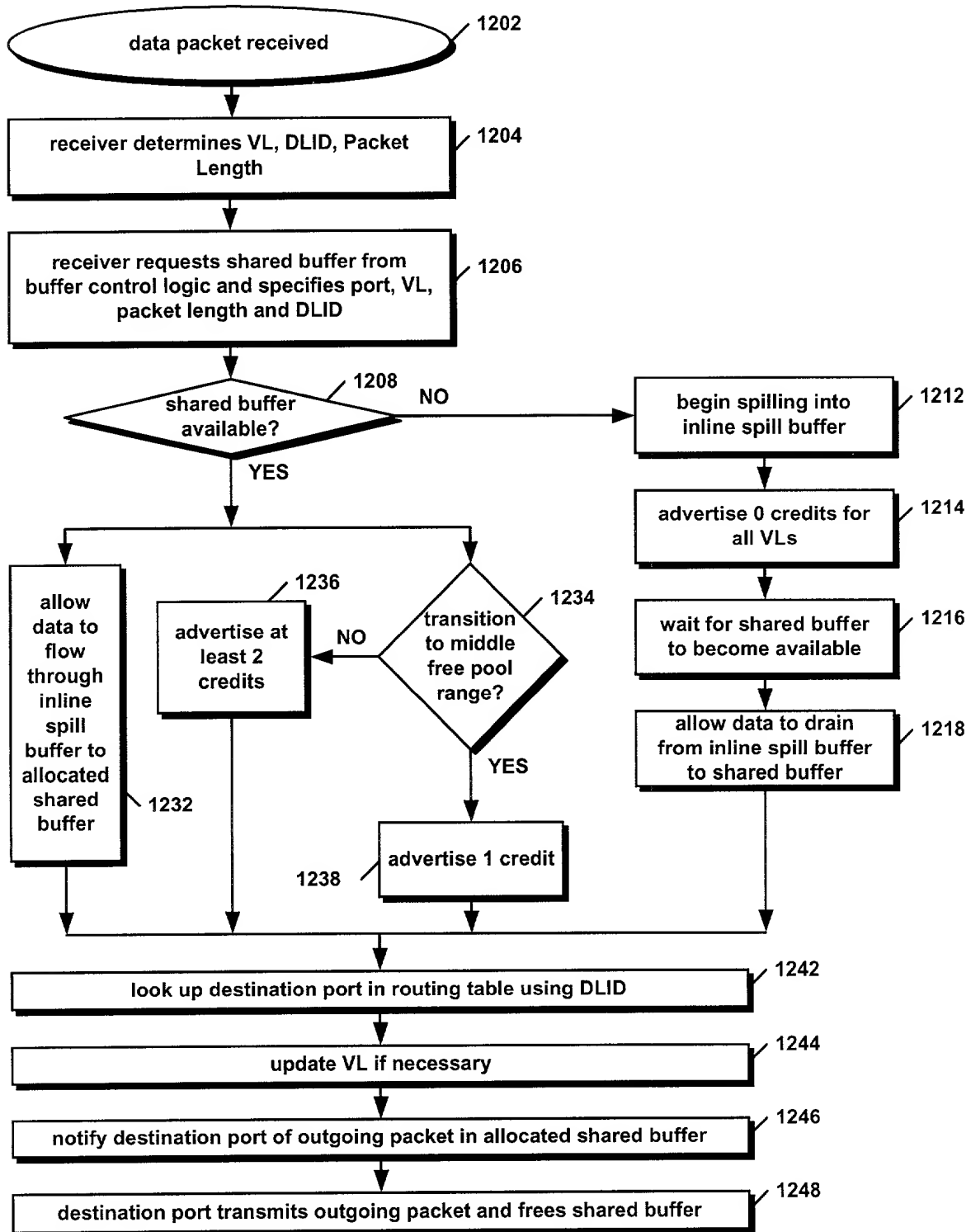
Timing Diagram For Determining Shutdown Latency

FIG. 11



Initialization

FIG. 12



Over-Advertising Flow Control

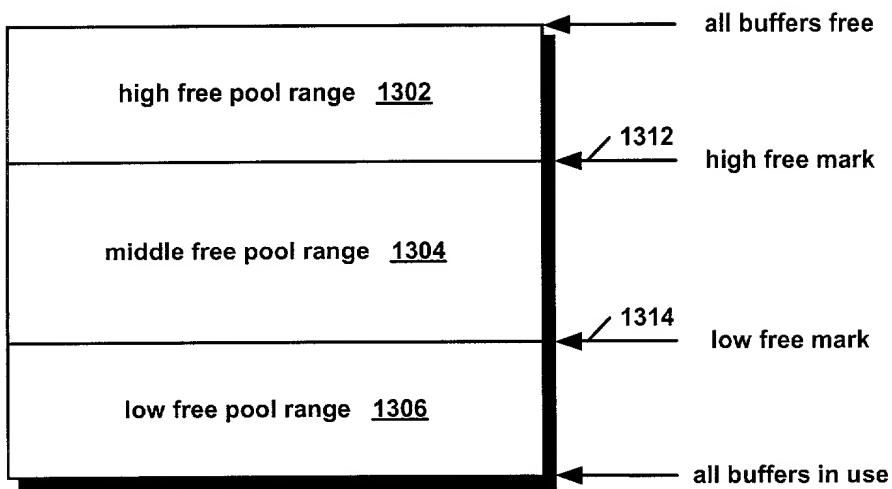


FIG. 13

Shared Buffer Free Pool Ranges

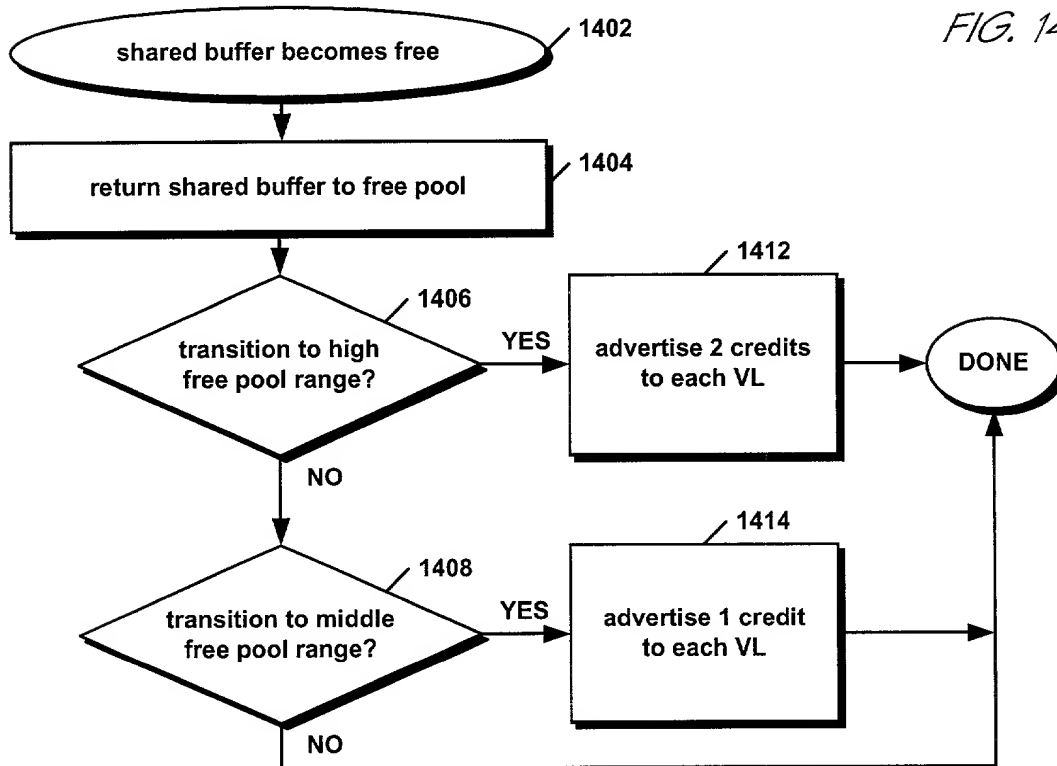
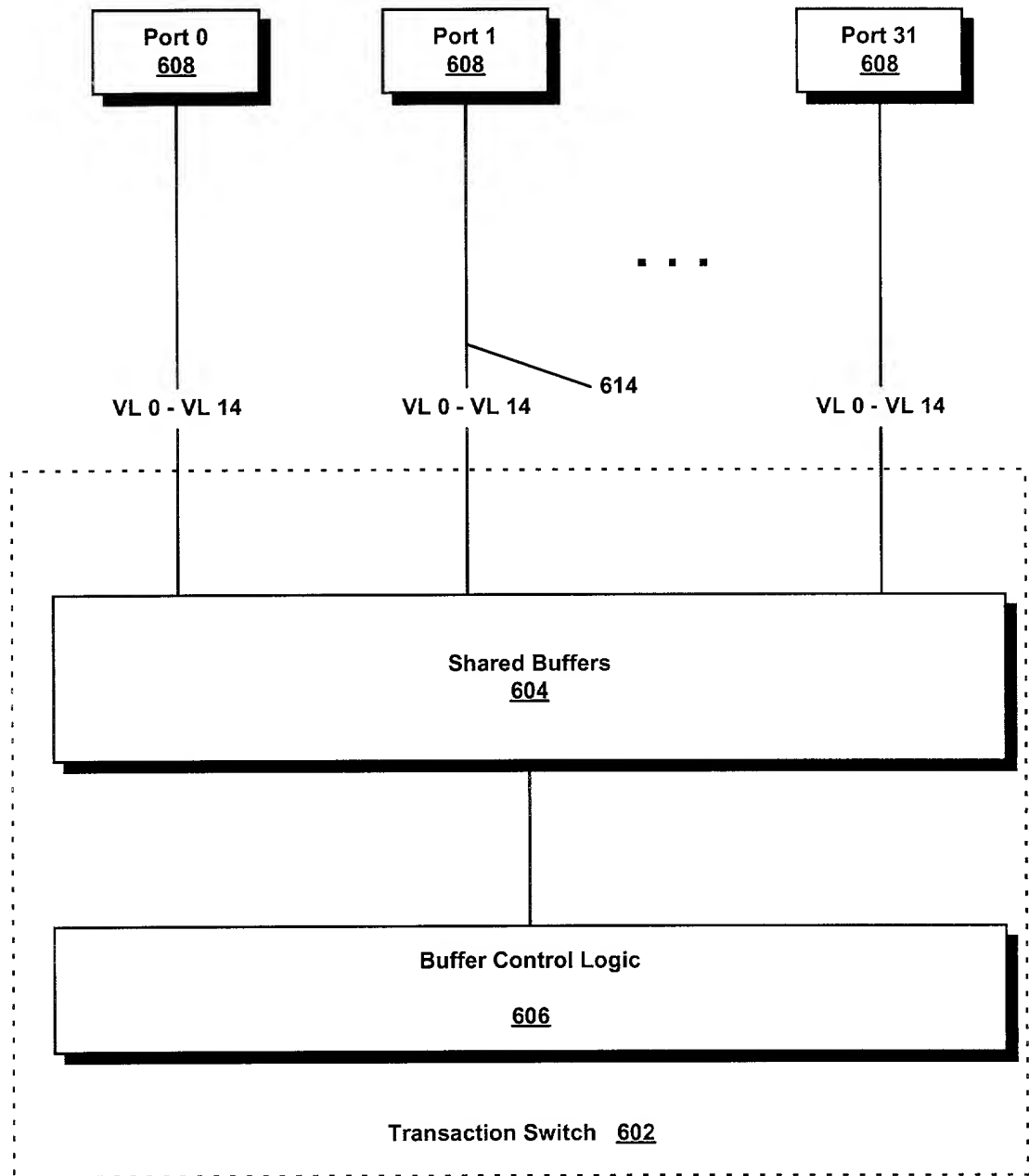


FIG. 14

Shared Buffer Free Action

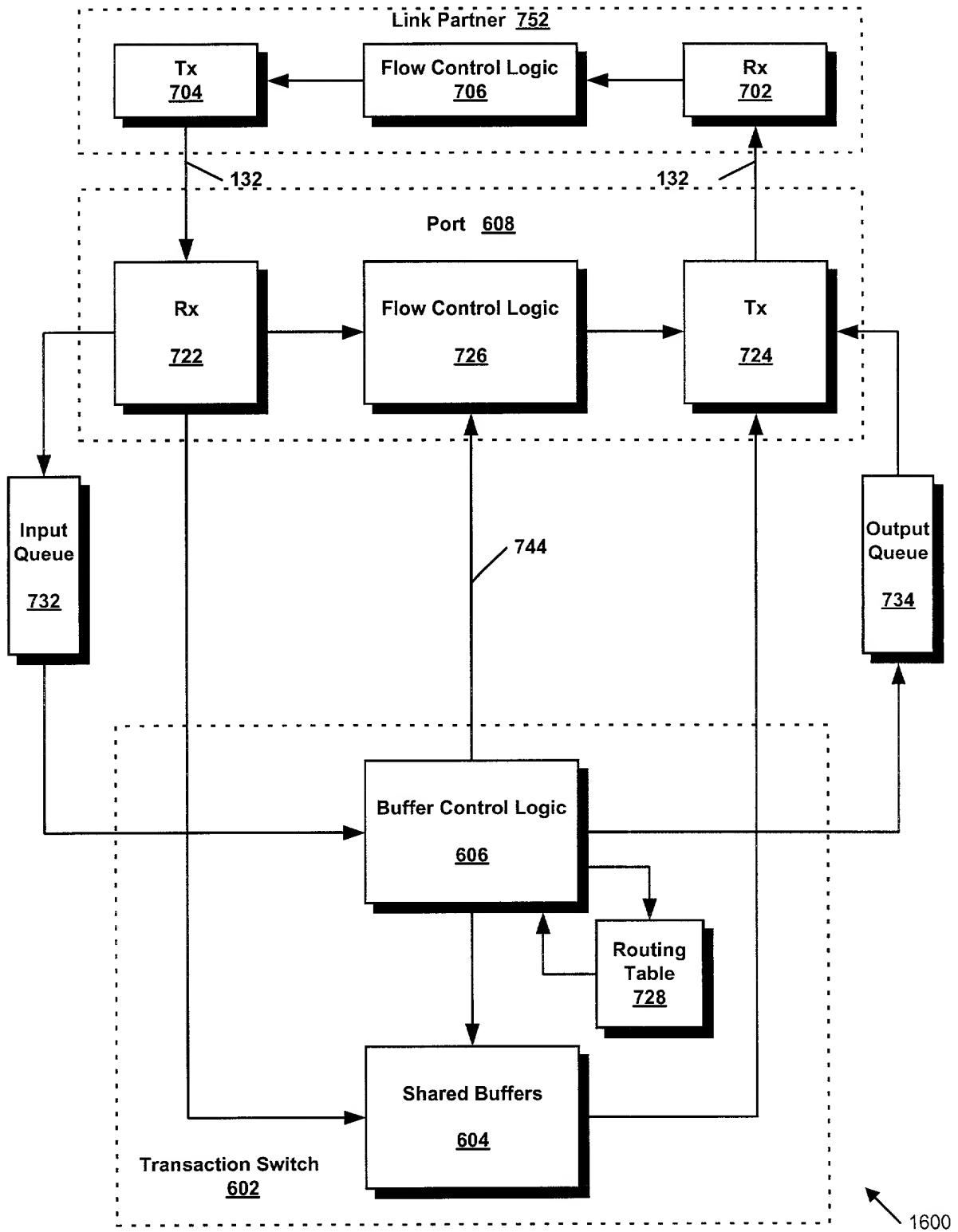
FIG. 15



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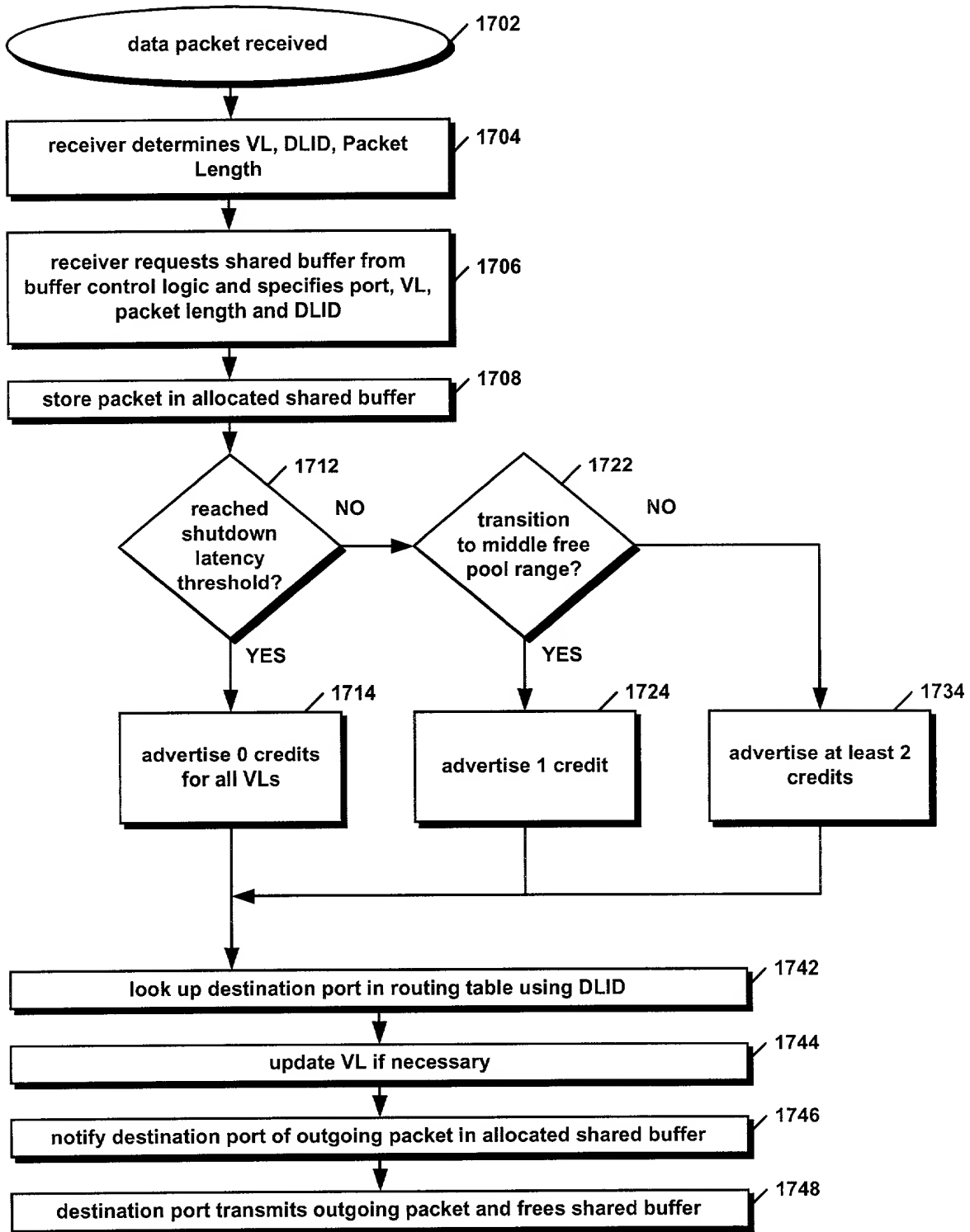
IB Switch Capable of Over-Advertising Buffering Resources Without Inline Spill Buffer

FIG. 16



Packet Buffering System Without Inline Spill Buffer

FIG. 17



Over-Advertising Flow Control

